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towards Tb/s routing in optical interconnects
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1 Executive Summary

This document provides the final component- and system-level specifications of PLATON's 2x2 and 4x4 routing platforms and an overview of the most recent system-level experimental evaluation activities. It includes the specifications for all specific PLATON router sub-blocks, like:

- Silicon-on-Insulator (SOI) platform
- Waveguides (Silicon waveguides and Dielectric Loaded – Surface Plasmon Polariton (DLSPP) waveguides)
- Interfaces (fiber-to-Silicon, Silicon-to-DLSPP, electrical)
- Silicon-on-Insulator Multiplexing (MUX) circuit
- Header detection / photodiode
- IC electronic control circuitry
- 2x2 Dielectric Loaded – Surface Plasmon Polariton (DLSPP) switching element
- 4x4 Dielectric Loaded – Surface Plasmon Polariton (DLSPP) switching matrix
- Network Traffic and Data formats
- Final 2x2 PLATON routing platform
- Final 4x4 PLATON routing platform

The logical and physical design of the 2x2 and 4x4 PLATON router systems has been completed for almost all the router sub-blocks.

2 Introduction

2.1 Purpose of this document

The objective of this deliverable is to provide the component- and system-level specifications for the final 2x2 and 4x4 PLATON router prototypes. It aims to provide an update on the specifications presented in deliverable D2.1 exploiting results that have been obtained within the project so far.

2.2 Document structure

The present deliverable is split into eight major chapters:

- Overview of PLATON routing concept
- Network Traffic and Data Formats
- Specifications for SOI platform, waveguides and interfaces
- PLATON component specifications
- Specifications for 2x2 PLATON routing platform

- Specifications for 4x4 PLATON routing platform
- Comparison with state-of-the-art routers for interconnects
- Experimental evaluation

2.3 Audience

This document is public.

3 Overview of PLATON routing concept

Both the 2x2 and 4x4 PLATON routing platforms operate with optical data line-rates of 40Gb/s and reside on a Silicon-on-Insulator Motherboard that hosts all the heterogeneous technologies, namely SOI-based components, Dielectric Loaded Surface Plasmon Polariton (DLSPP) switches, Photodiodes and Integrated Circuit Microcontrollers. The 2x2 router offers an aggregate switching throughput of 560 Gb/s, whereas the 4x4 router provides a total throughput of 1.12 Tb/s. Briefly the role of each router sub-unit is as follows:

1. 7x1 SOI MUX (Multiplexer): This subsystem is used to multiplex the 7 incoming 40Gb/s data traffic carrying wavelengths into a common, single optical traffic stream that will follow the same route through the network. Two and four 7x1 SOI multiplexing modules will be employed in the 2x2 and 4x4 PLATON router platforms, respectively. The SOI MUX will rely on silicon-based photonic integrated components.

2. PD O/E Conversion Stage: Photodiodes integrated on the SOI motherboard will form the O/E conversion stage of the routing platform. PDs will be used for converting the optical header information into respective electrical header pulses to be subsequently processed by the IC Header Processing and Control Circuit. One PD will be employed for every header wavelength, which in turn implies that in the case of the 2x2 and 4x4 router a total number of 2 and 4 PDs will be used, respectively.

3. IC Header Processing and Control Circuit: This subsystem is used for processing the incoming header information and for generating the appropriate electrical control signals that will drive the DLSPP switching matrix. For the 2x2 router, the IC circuit will have two input ports for receiving the respective electrical header pulse streams and will provide two electrical output signals for controlling the state of the 2x2 switching matrix. In the case of the 4x4 router, the IC circuit will incorporate four input and eight output ports.

4. DLSPP switching matrix: The DLSPP switching matrix routes the incoming traffic streams towards the different outputs depending on the header information. PLATON's switching matrix will rely on Dielectric Loaded Surface Plasmon Polariton (DLSPP)-based thermo-optic switching elements. A 2x2 switching matrix will be used for the 2x2 routing platform, whereas a 4x4 switching matrix consisting of multiple interconnected 2x2 switching structures will be used for the 4x4 PLATON router.

4 Network Traffic and Data Formats

Every traffic stream will comprise 8 wavelengths, 7 of them carrying useful data and one wavelength carrying the header information. This format is fully compliant with optical interconnect applications as each wavelength can be considered as the traffic generated by a respective BladeCard.

1. Data wavelengths: For both the 2x2 and the 4x4 PLATON router demonstrations, the 7 data wavelengths will carry packet-formatted Non-Return-to-Zero (NRZ) traffic at 40Gb/s, with packets that correspond to different wavelengths overlapping in time. A low channel spacing of 100GHz is targeted between the different wavelengths in order to allow for maximum bandwidth utilization occupying a total spectral region of 600GHz, whilst ensuring effective spectral discrimination between the different 40Gb/s channels. The requirement for reserving the minimum possible total bandwidth for the 7 data wavelengths is a crucial factor also towards minimizing the wavelength dependence of the switching performance, given that all wavelengths belonging to the same input traffic stream will have to reside within the bandwidth of a single DLSP-based interferometric switch in order to emerge at the same router output port. The total duration of each packet will be 1µsec, suggesting that each packet will deliver a total amount of 5kbytes of 40Gb/s data. Guardband intervals between successive packets will be incorporated, with their duration depending on the rise- and fall-times of the DLSP thermo-optic response. A total guardband duration of less than 250nsec is targeted.

2. Header wavelength: For both the 2x2 and the 4x4 PLATON router demonstrations, the header wavelength will be spaced 100GHz from the 7th and last data wavelength and will carry all the necessary address information that will dictate the route of the total incoming 7-wavelength traffic stream. In the case of the 2x2 router where a decision between two output ports has to be made for each incoming traffic stream, the header information will incorporate two header pulses within a 1µsec interval, suggesting that each header pulse will have a time duration of 500nsec. In the case of the 4x4 router where 4 output ports will be available, the header will comprise 3 pulses within the 1µsec packet duration, implying a header pulse duration of 330nsec. A burst-switching approach will be adopted for the header and data synchronization scheme, with the header information being timely mistuned compared to the respective data packets so as to ensure enough available time for header processing in the IC circuitry. This scheme relaxes the need for delaying or storing the 40Gb/s data packets during switch state determination.

Table 1: Header Content for 2x2 routing

Header	Bit#1	Bit#2	Header Content Interpretation
H1	0	0	No packet present
	0	1	Exits through Router Out#1 (BAR state) when entering through In#1
	1	0	Exits through Router Out#2 (CROSS State) when entering through

			In#1
H2	0	0	No packet present
	0	1	Exits through Router Out#2 (BAR state) when entering through In#2
	1	0	Exits through Router Out#1 (CROSS State) when entering through In#2

Table 2: Traffic & Data Specifications for 2x2 Routing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Wavelength	λ_1		1534		nm
Data Wavelength	λ_2		1534,8		nm
Data Wavelength	λ_3		1535,6		nm
Data Wavelength	λ_4		1536,4		nm
Data Wavelength	λ_5		1537,2		nm
Data Wavelength	λ_6		1538		nm
Data Wavelength	λ_7		1538,8		nm
Data Wavelength	λ_8		1540,8		nm
Data Wavelength	λ_9		1541,6		nm
Data Wavelength	λ_{10}		1542,4		nm
Data Wavelength	λ_{11}		1543,2		nm
Data Wavelength	λ_{12}		1544		nm
Data Wavelength	λ_{13}		1544,8		nm
Data Wavelength	λ_{14}		1545,6		nm
Header Wavelength	λ_{H1}		1539,6		nm
Header Wavelength	λ_{H2}		1546,4		nm
Data channel spacing	Δf		100		GHz
Data-Header channel spacing	Δf		100		GHz
Data pulse format			NRZ		
Data line-rate	B		40		Gb/s
Data packet size			5		kbyte
Data packet duration	T_p		1		μ sec
Guardband duration	T_G			0.25	μ sec
Header-Data Offset time			0.5		μ sec
Header Line-rate			2		MHz
Header Size			2		bits
Header Pulse format			NRZ		
Header Pulse Duration			0.5		μ sec

Similar parameter specifications will be used for the network traffic employed in the 4x4 routing scenario. The main differences compared to the 2x2 routing scenario will be:

- A total set of 4 incoming traffic streams will be used, suggesting that four sets of 7-wavelength packet traffic will be employed. This means that besides λ_1 - λ_7 and λ_8 - λ_{15} already used in the case of 2x2 routing, two new wavelength groups of λ_{16} - λ_{23} and λ_{24} - λ_{31} will be incorporated. In addition, two new header wavelengths λ_{H3} and λ_{H4} will be used for designating the address information for traffic streams #3 and #4, respectively. The exact values of all these wavelengths are provided in Table 5 below.
- The Header information will employ three consecutive bits, given that in the case of 4x4 routing a total number of 4 possible input-output combinations can be selected.

Table 3: Header Content for 4x4 routing

Header	Bit#1	Bit#2	Bit#3	Header Content Interpretation
H (irrespective of traffic stream number)	0	0	0	No packet present
	0	0	1	Exits through Router Out#1
	0	1	0	Exits through Router Out#2
	0	1	1	Exits through Router Out#3
	1	0	0	Exits through Router Out#4

Table 4: Header Specifications for 4x4 Routing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Header Line-rate			3		MHz
Header Size			3		bits
Header Duration			1		μ sec
Header Pulse format			NRZ		
Header Pulse Duration			0.333		μ sec

Table 5: Traffic & Data Specifications for 4x4 Routing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Wavelength	λ_1		1534		nm
Data Wavelength	λ_2		1534,8		nm
Data Wavelength	λ_3		1535,6		nm
Data Wavelength	λ_4		1536,4		nm
Data Wavelength	λ_5		1537,2		nm
Data Wavelength	λ_6		1538		nm
Data Wavelength	λ_7		1538,8		nm
Data Wavelength	λ_8		1540,8		nm
Data Wavelength	λ_9		1541,6		nm
Data Wavelength	λ_{10}		1542,4		nm
Data Wavelength	λ_{11}		1543,2		nm
Data Wavelength	λ_{12}		1544		nm
Data Wavelength	λ_{13}		1544,8		nm
Data Wavelength	λ_{14}		1545,6		nm
Data Wavelength	λ_{15}		1547,7		nm
Data Wavelength	λ_{16}		1548,5		nm
Data Wavelength	λ_{17}		1549,3		nm
Data Wavelength	λ_{18}		1550,1		nm
Data Wavelength	λ_{19}		1550,9		nm
Data Wavelength	λ_{20}		1551,7		nm
Data Wavelength	λ_{21}		1552,5		nm
Data Wavelength	λ_{22}		1557		nm
Data Wavelength	λ_{23}		1557,8		nm
Data Wavelength	λ_{24}		1558,6		nm
Data Wavelength	λ_{25}		1559,4		nm
Data Wavelength	λ_{26}		1560,2		nm
Data Wavelength	λ_{27}		1561		nm
Data Wavelength	λ_{28}		1561,8		nm
Header Wavelength	λ_{H1}		1539,6		nm
Header Wavelength	λ_{H2}		1546,4		nm
Header Wavelength	λ_{H3}		1553,3		nm
Header Wavelength	λ_{H4}		1562,6		nm

5 Final specifications for SOI platform, waveguides and interfaces

5.1 SOI platform

PLATON's 2x2 and 4x4 router platforms will be realized on a Silicon-on-Insulator (SOI) motherboard chip that will contain silicon nanophotonic elements (waveguides, couplers, multiplexing circuitry and photodetectors) and will be at the same time capable of hosting the plasmonic switching elements and the IC control circuitry. The SOI motherboard will involve:

- a. **Optical 7X1 MUX circuitry** capable of multiplexing up to 7 optical data wavelengths with 100GHz channel spacing into a single waveguide.
- b. **Monolithically integrated Photodiodes** that will be used for the optoelectronic conversion of the packet-rate header pulses in order to drive the IC micro-controller circuit with the electrical header information.
- c. **A gold lift-off chip area to enable subsequent DLSP waveguide writing processes**, so as to allow for the incorporation of the DLSP-based switching matrix.
- d. **A chip-area for hosting the hybridly integrated IC microcontroller circuit.**
- e. **Metal interconnects** for guiding the electrical-RF signals inserted into or generated by the IC circuit and for thermal tuning of the SOI MUX circuitry.

5.2 Silicon waveguides

The rib Si waveguide dimensions for PLATON have been defined to be 340nm height, 400nm width and 50nm slab height on top of a 2 μ m SOI BOX and coated with 800nm thickness SOG. The dimensions have been numerically and experimentally tested to allow for TM polarization mode propagation with losses lower than 3dB/cm.

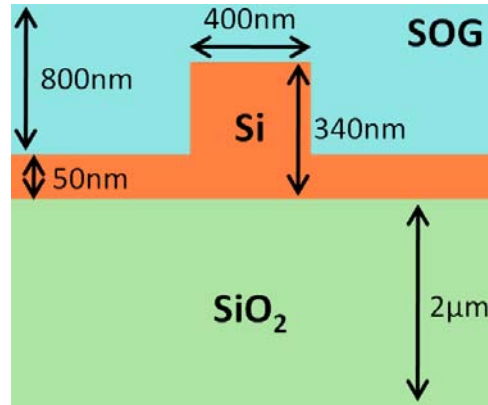


Figure 5.1: Cross-section of the Si-waveguide structure

Table 6: Silicon waveguide specifications

Parameter	Symbol	Typ.	Unit
SiO ₂ Box Height	H _{SiO₂}	2	μm
Si waveguide width	W	400	nm
Si waveguide height	H	340	nm
Si slab height	h	50	nm
SOG coat thickness	T	800	nm
TE Propagation losses @1550nm	α _{TE}	2.5-4.5	dB/cm
TM Propagation losses @1550nm	α _{TM}	2.5-4.5	dB/cm
TE and TM Propagation @1550nm		Single mode	

5.3 DLSP waveguides

Table 7 presents the optimum DLSP waveguide dimensions and characteristics that will be employed in the final thermo-optic DLSP switching elements.

Table 7: DLSP waveguide specifications

Parameter	Symbol	Typ.	Unit
Polymer Height	H	600	nm
Polymer width	W	500	nm
Polymer type	Cycloaliphatic acrylate polymer		
Polymer refractive index @1550nm		1.505	
Polymer thermo-optic coefficient	TOC	-2.9x10 ⁻⁴	K ⁻¹

Gold film height	H_{Au}	60	nm
Gold film width	W_{Au}	3	μm
Propagation losses @1550nm	α	0.1	dB/ μm
Propagation Length (1/e damping) @1550nm	L_{sp}	44	μm
Mode effective index @1550nm	N_{eff}	1.237	

5.4 Fiber-to-Silicon coupling interfaces

PLATON's final 2x2 and 4x4 routing platforms will employ high-index contrast TM grating-based vertical coupling structures. Table 8 shows some important specifications of the new fully-etched TM grating coupler design to be finally adopted in PLATON.

Table 8: Grating-based vertical fiber-to-Si coupling structure specifications

Parameter	Symbol	Typ.	Unit
Number of periods	N	22	
Grating period	Λ	0.7	μm
Grating width		12	μm
Etch depth		290	nm
Vertical distance	S	1.3	μm
Coupling length	L_c	3.68	μm
Filling factor	ff	0.8	
Pitch		0.355	μm
Incidence angle	θ	10	deg
Insertion losses	α_L	3	dB
Bandwidth	BW	55	nm
1dB loss alignment tolerance		± 2	μm

5.5 Silicon-to-DLSPP coupling interfaces

The Si-DLSPP interface losses were experimentally measured and were found to be $\sim 2.4\text{dB}$, i.e. very close to the theoretically expected performance. main specifications for the DLSPP-to-Si-rib transition interfaces are summarized in Table 9.

Table 9: DLSPP-to-Si and Si-to-DLSPP interface specifications

Parameter	Symbol	Typ.	Unit
Si-taper initial width	W1	400	nm

Si-taper end width	W ₂	175	nm
Si-taper length	L _t	10	μm
Metal gap	L _G	0.5	μm
Vertical Offset	H _{offset}	0	nm
Losses	α	2.4	dB

6 PLATON component specifications

6.1 Silicon-on-Insulator Multiplexing (MUX) circuit

MUX circuitry will rely on an interconnected arrangement of 7 microring-based SOI structures. An overview of the targeted specifications is provided below:

Table 10: 7x1 SOI MUX specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
No# of Input ports			7		
No# of Output ports			1		
Si Rib Width	W		400		nm
Si Rib Height	H		340		nm
Si Rib Slab	h		50		nm
Si waveguide Top-Cladding			SOG Accuglass T512B		
Material for electrical contacts			Titanium		
Thickness of electrical contacts	W _{Ti}		100		nm
Operating Wavelength Range		1500		1600	nm
Center Wavelength		1530	1550 (depending on the channel band selected)	1570	nm
Channel spacing	Δf		100		GHz
Channel 3-dB bandwidth	$\Delta \lambda$		0.32		nm
Footprint / Chip size (w)x(L) (without the electrical contacts)			50x350		μm ²
Footprint / Chip size (w)x(L) (including electrical contacts)			150x350		μm ²
Power loss per channel	α		0.5	1	dB
Channel Crosstalk		-35	-20	-15	dB
Power consumption per			1		mW/K

temperature deviation					
Maximum Heating power per heating element		10		100	mW

6.2 Header detection / photodiode

All-silicon photodetectors will be employed in PLATON as they can fulfill its requirements by providing the best compromise for easy, cost-effective integration and low-rate pulse detection. The targeted specifications for the photodetector option used in the final 2x2 and 4x4 router platforms are summarized in the following table:

Table 11: Header O/E Conversion: Photodiode specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
Footprint			0.1		mm ²
Photodiode Reverse Voltage	V_{PD}		3		V
Operating Wavelength Range	λ	1500		1600	nm
DC Responsivity @1550nm	R		0.1		A/W
3-dB cut-off frequency	f_{3dB}		1		GHz
Photodiode Dark Current	I_{dark}			100	nA

6.3 IC electronic control circuitry

The digital control IC will be responsible for processing the header information and for controlling the output DLSPP switches according to a pre-defined routing look-up table. The routing look-up tables for both the 2x2 and the 4x4 PLATON routers have been presented in Deliverable D2.1 on "Specifications of PLATON's 2x2 and 4x4 routing platforms". The respective IC circuits have been deployed in FPGA boards showing successful operation with respect to PLATON router requirements.

A summary of the IC microcontroller specifications is provided below:

Table 12: Specifications of digital control IC

Parameter	Description/Value
Technology	Austriamicrosystems C35B4C3
Clock Speed	up to 20 MHz
Input/Output - Options	3.3V (supply voltage - VDD) digital CMOS signals
	0.7 VDD input high level
	0.7 VDD input low level
	2 inputs/2 outputs for 2x2 router
	4 inputs/8 outputs for 4x4 router
	Bidirectional CMOS buffers up to 24mA
	Bidirectional Schmit-Trigger buffers up to 24mA
	Bidirectional TTL buffers up to 24mA
Tri-State output buffers up to 24mA	

Footprint/Dimensions	4x4 mm ²
Latency	0.5 μsec
Assembly	Wire bonding / Flip-chip

6.4 Metal Interconnects

The metal interconnects will provide signal and power distribution between the components. Their design will rely on impedance controlled layouts so as to maximize the power delivered to the modulators and control the timing of the header signaling for the IC Microcontroller. In order to reduce the number of required metallization levels single metallization layer configurations will be employed. Initial designs for different TML configurations (Coplanar Waveguide, Coplanar Strips) and substrate build-ups (metal layer on BOX, metal layer on redistribution layer RDL) have been done based on numerical simulations. The electrical characteristics are compiled in Table 13. The designs take into account the different geometrical features of the processes.

Table 13: Specifications for PLATON's electrical interconnects

Parameter	Symbol	TML on BOX	TML on RDL	Unit
CPW width of center conductor	Wcpw	15	100	um
CPW gap signal to ground	Gcpw	1	5	um
CPS width of signal conductors	Wcps	15	45	um
CPS gap between signal lines	Gcps	5	10	um

The metal interconnects will be deployed using:

- Alu metallization with 500nm thickness ($\sim 3 \times 10^{-6}$ Ohmcm)
- top-cladding with thickness between 100-1500 nm
- Via etching down to the silicon layer
- Via etching down to the heater layer

For chip scale fabrication, photolithography with $\sim 5\mu\text{m}$ alignment accuracy and $\sim 5\mu\text{m}$ minimum feature size will be used.

6.5 2x2 Dielectric Loaded – Surface Plasmon Polariton (DLSP) switching matrix

The specifications for the 2x2 DLSP switch are summarized in Table 14:

Table 14: 2x2 DLSP Switching Matrix Specifications

Parameter	Symbol	Switch	Unit
No. of ports (input x output)		4 (2/2)	
No. of switching elements		1	
Waveguide Type		DLSP-W	
Operating Wavelength Region	λ	1500-1600	nm
Free Spectral Range	FSR	>100	nm
Channel Bandwidth	$\Delta\lambda_{3dB}$	>60	nm
Cross-section (waveguide mode) dimensions		0.5x0.6	μm^2
Footprint / Chip size (w)x(L)		15x40	μm^2
Total power consumption	P_{elec}	8	mW
Optical Power Losses (input/output)	α	5	dB
Latency	$t_{latency}$	220	fsec
Switching time	Δt_{speed}	1	μsec
Optical Crosstalk	ER	<-20	dB

6.6 4x4 Dielectric Loaded – Surface Plasmon Polariton (DLSP) switching matrix

The targeted specifications are summarized in the following table:

Table 15: 4x4 DLSP Switching Matrix Specifications

Parameter	Symbol	MZI-based 4x4 matrix	Unit
No. of ports (input x output)		8 (4/4)	
No. of switching elements		4	
Waveguide Type		DLSP-W	
Optical Bandwidth	$\Delta\lambda$	>100	nm
Operating Wavelength Region	λ	1500-1600	
Free Spectral Range	FSR	>100	nm
Channel Bandwidth	$\Delta\lambda_{3dB}$	>60	nm
Cross-section (waveguide mode) dimensions		0.5x0.6	μm^2
Footprint / Chip size (w)x(L)		60x150	μm^2
Total power consumption	P_{elec}	<35	mW
Optical Power Losses (input/output)	α	10	dB

Latency	t_{latency}	<0.75	psec
Switching time	Δt_{speed}	1	μsec
Optical Crosstalk	ER	<-20	dB

7 Final specifications for 2x2 PLATON routing platform

The targeted specification for the 2x2 PLATON router are provided in the table below:

Table 16: PLATON 2x2 Router Specifications

Parameter	Symbol	Asymmetric MZI-based 2x2 router	Unit
Chip throughput		560	Gb/s
No. of input/output ports		16/2	
Line rate / input port		40	Gb/s
Line rate / output port		280	Gb/s
Operating Wavelength Range	λ	1500-1600	nm
Total power consumption	P_{elec}	<2.5	W
Chip size (w)x(L)		up to full 6" wafer	
Losses (non-pigtailed chip)	α_{chip}	~ 8	dB
Losses (fiber-pigtailed chip)	α	~ 14	dB
Latency (port-to-port)	$t_{latency}$	<1	psec
Extinction Ratio	ER	>25	dB
Packet size @line rate		5	KBytes

8 Final specifications for 4x4 PLATON routing platform

The targeted specifications for the 4x4 PLATON router are provided in the table below:

Table 17: PLATON 4x4 Router Specifications

Parameter	Symbol	MZI-based 4x4 router	Unit
Chip throughput		1.12	Tb/s
No. of input/output ports		32/4	
Line rate / input port		40	Gb/s
Line rate / output port		280	Gb/s
Operating Wavelength Range	λ	1500-1600	nm
Total power consumption	P_{elec}	<4	W
Chip size (w)x(L)		up to full 6" wafer	
Losses (non-pigtailed chip)	α_{chip}	~ 16 dB	dB
Losses (fiber-pigtailed chip)	α	~ 22 dB	dB
Latency (port-to-port)	$t_{latency}$	<1.5	psec
Extinction Ratio	ER	>15	dB
Packet size @line rate		5	KBytes

9 Conclusions

This deliverable is the final specification sheet of PLATON's 2x2 and 4x4 routing platforms. The requirements from the system point of view have been updated regarding deliverable D2.1 and translated into detailed electrical, optical and mechanical specifications.